Re "112" Rejections

Examiner rejected claims 1-12 under 35 USC 112, second paragraph, as being indefinite.

To overcome these rejections, Applicant amends his claims as follows.

In claim 1, line 15, the word "substantively" is replaced with the word --substantially--.

In claim 11, line 21, the term "transistor, but" is replaced with the word --transistor--.

In claim 12, line 18, the term --a-- is inserted immediately before the word "part".

Examiner finds claims 2, 3 and 7 to be indefinite because the terms "one tenth" or the indicated time durations "such as 2, 8 or 32 microseconds" have no antecedence in the specification.

To remedy this situation, immediately after the second paragraph at page 6 of the specification, the following paragraph is added:

--The fundamental frequency of the voltages and currents illustrated by the waveforms of Fig. 3 is typically in the range of 20-40 kHz; which means that the duration of a complete waveform cycle is in the range of 25-50 micro-seconds. Thus, if the total period were to have a duration of 32 micro-seconds, the duration of each of the six time-segments identified with Roman numerals I through VI would be about 5.33 micro-seconds.--

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Aside from the above comments, with particular reference to claim 2, it is clear from direct inspection of Fig. 3A (which depicts the inverter voltage) that:

"the duration of the first period is shorter than half the duration of the fundamental period by at least one tenth".

In fact, as plainly shown in Fig. 3A, "the duration of the first period is shorter than half the duration of the fundamental period" by a about one third.

Re "102" Rejections

Examiner rejected claims 1, 4-6 and 8-12 under 35 USC 102b as being clearly anticipated by Walker.

Applicant traverses these rejections for the following reasons.

(a) Exemplary claim 1 includes:

"inverter means ... operative to provide an inverter voltage ... characterized by: ... (ii) having a fundamental period; (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level; (iv) the duration of the first period being substantially equal to that of the second period; ... and (vi) the duration of the first period being substantially shorter than half the duration of the fundamental period". (Emphasis added)

This feature is neither disclosed nor suggested by Walker.

On the contrary.

With reference to his Fig. 1, Walker expressly refers to a "Square Wave Oscillator". Also, in his column 2, lines 4-5, he states that: "the AC source produces a substantially square wave".

In the IEEE Standard Dictionary of Electrical and Electronics Terms (Second Edition), the term "square wave" is defined as follows:

"A periodic wave that alternately for equal lengths of time assumes one of two fixed values, the time of transition being negligible in comparison".

Of course, with reference to the terminology used in exemplary claim 1, in case of a square wave voltage, "the duration of the first period" would have been substantially equal to (and definitely not substantially shorter than) "half the duration of the fundamental period".

(b) Clearly, the invention claimed by Applicant pertains to an inverter-type electronic ballast wherein the inverter provides an output voltage characterized -- for instance -- as having a trapezoidal waveform as differentiated from a square waveform. That is, in direct contrast with a squarewave voltage (as defined by the IEEE Dictionary), the output voltage of the inverter in Applicant's invention provides for a "time of transition" that is deliberately not "negligible in comparison".

This type of waveform can not be considered obvious to use in an inverter-type ballast for the reason that the attainment of this type of waveform -- which might be achieved via intentionally slow and gradual switching of the inverter transistors (i.e., by way of so-called Class B operation) -- would entail prohibitively high transistor dissipation.

(c) Claim 5 defines an arrangement wherein:

"during each fundamental period, the periodically conducting transistor conducts in a forward direction for a first conduction period; the first conduction period having a duration substantially shorter than the duration of the first period".

This feature is neither described nor suggested by Walker.

Applicant can find no disclosure in Walker to the effect that one of his periodically conducting transistors conducts in the forward direction for a "period having a duration substantially shorter than the duration of the first period" -- especially in view of the fact that this "first period" is "substantially shorter than half the fundamental period".

Re "103" Rejections

Examiner rejected claims 2-3 and 7 under 35 USC 103 as being unpatentable over Walker.

Applicant traverses these rejections for the various reasons presented hereinabove in connection with Applicant's traversal of Examiner's "102" rejection of parent claim 1. To those reasons, Applicant adds the following reasons.

(d) Claim 2 defines an arrangement wherein:

"the duration of the first period is shorter than half of the duration of the fundamental period by at least one tenth".

This feature is not in any way suggested by Walker.

Walker plainly discloses an arrangement wherein the inverter's output voltage is a squarewave voltage; in which case the duration of the first period is <u>not</u> shorter than half the duration of the fundamental period, especially not by "one tenth". He provides no hint whasoever to the effect that it might be functional or even desirable to provide an inverter output voltage of some other waveshape.

(e) The reasons provided in connection with claim 2 pertain to claims 3 and 7 as well.

Re the Claims

In the third line of claim 5, replace the word "for" with the words --only during--.